What is claimed is:

1. A semiconductor apparatus, comprising:

a semiconductor integrated circuit which comprises a conductive pattern;

an insulating layer which is formed on the semiconductor integrated circuit to forms a plurality of base members having uneven heights;

an opening which is formed through the insulating layer to expose a part of the conductive pattern; and

a conductive layer which is formed on the insulating layer and the opening, the conductive layer is extending from the exposed portion of the conductive pattern to the top surface of the highest base member, wherein

an electrode is composed of the insulating layer, the opening and the conductive layer.

2. The semiconductor apparatus, according to claim 1, wherein

the highest base member is formed in one united body with the other base members.

3. The semiconductor apparatus, according to claim 2, wherein

the other base members are formed to have exposed top surfaces.

4. The semiconductor apparatus, according to claim 1, wherein

the highest base member is formed to have an exposed portion on a side surface.

5. The semiconductor apparatus, according to claim 1, wherein the opening is formed to surround the highest base member.

6. The semiconductor apparatus, according to claim 1, wherein the insulating layer functions as a protection layer of the semiconductor integrated circuit.

7. The semiconductor apparatus, according to claim 1, further comprising:

a bump electrode which is formed on the conductive layer at the top surface of the highest base member.

8. The semiconductor apparatus, according to claim 1, further comprising:

the insulating layer is made of polyimide resin.

9. The semiconductor apparatus, according to claim 1, wherein the conductive layer is selected from a single layer mainly composed of gold (Au), a single layer mainly composed of copper (Cu), a single layer mainly composed of lead (Pb) and tin (Sn) and an integrated layer mainly composed of gold (Au).

10. A semiconductor apparatus, comprising:

a semiconductor substrate which comprises a semiconductor integrated circuit, and an electrode, which is composed of a base member of

insulating material formed on the semiconductor integrated circuit and a conductive layer formed on the surface of the base member;

a connection substrate on which the semiconductor substrate is mounted with a face-down technique; and

a seal member which is filled in the space between the semiconductor substrate and the connection substrate, wherein

the base member and the seal member are made of the same material.

11. The semiconductor apparatus, according to claim 1, further comprising:

a connection substrate on which the semiconductor integrated circuit with the electrode is mounted with a face-down technique; and

a seal member which is filled in the space between the semiconductor integrated circuit and the connection substrate, wherein

the base member and the seal member are made of the same material.

12. A method for fabricating a semiconductor apparatus, comprising the steps of:

providing a semiconductor integrated circuit comprising a conductive pattern;

forming an insulating layer on the semiconductor integrated circuit;

forming an opening through the insulating layer to expose a part of the conductive pattern;

forming a conductive layer over the insulating layer with the opening;

patterning the conductive layer except a portion extending from the exposed part of the conductive pattern to a predetermined portion of the insulating layer; and

shaping the insulating layer at the portion uncovered with the conductive layer to have a height lower than the portion covered with the conductive layer.

13. The method, according to claim 12, wherein

the step for forming the opening comprises the steps of:

(1)coating hardenable resin over the semiconductor integrated circuit to form the insulating layer;

(2)forming the opening through the hardenable resin; and

(3)hardening the resin.

14. The method, according to claim 12, wherein

the step for forming the opening comprises the steps of:

(1)coating photosensitive resin over the semiconductor integrated circuit to form the insulating layer; and

(2)forming the opening through the insulating layer with lithographic technique.

15. The method, according to claim 12, wherein

the step for forming the opening comprises the steps of:

(1)coating insulating resin over the semiconductor integrated circuit to form the insulating layer; and

(2)forming the opening through the insulating layer with laser machining technique.

16. The method, according to claim 12, wherein

the step for forming the opening comprises the steps of coating insulating resin over the semiconductor integrated circuit to form the insulating layer; and

the step for shaping insulating layer is the step of plasma-etching the insulating layer.

17. The method, according to claim 12, wherein

the insulating layer is of polyimide resin.

18. The method, according to claim 12, wherein

the insulating layer is formed on the semiconductor integrated circuit which is not covered with a protection layer so that the insulating layer functions as a protection layer.

19. The method, according to claim 12, further comprising the step of:

forming a bump electrode on the conductive layer, which is formed on the insulating layer.

20. The method, according to claim 12, further comprising the steps of:

performing an electrical test of the semiconductor integrated circuit; and

forming a pattern for trimming of the semiconductor integrated circuit before the steps of forming the insulating layer and forming the opening, wherein

the steps of forming the insulating layer and forming the opening are performed so that the insulating layer remains on the entire surface of the pattern for trimming.

21. A method for fabricating a semiconductor apparatus, comprising the steps of:

fabricating a semiconductor substrate which comprises a semiconductor integrated circuit, and an electrode, which is composed of a base member of insulating material formed on the semiconductor integrated circuit and a conductive layer formed on the surface of the base member;

placing the semiconductor substrate to face a connection substrate according to a face-down technique;

connecting the electrode to the connection substrate;

filling a seal member in the space between the semiconductor substrate and the connection substrate, wherein

the base member and the seal member are made of the same material.